

Syllabus for F.Y. B.Sc. (Electronics for Computer Science)
Paper II
Principles of Digital Electronics-I

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| Semester- I | Subject Code: BS11508 | Lectures: 40 |
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Objectives:

The syllabus aims in equipping students with

- Concepts of digital electronics
- Learning number systems and their representation
- Understanding logic gates, Boolean algebra and K-maps
- Studying arithmetic circuits

| Unit 1: Number Systems and Logic Gates | No. of Lect.=14 |
|--|-----------------|
| • Introduction to decimal, Binary, Octal and hexadecimal number systems and their inter conversions | 4 |
| • Unsigned, Signed and fractional binary number representations, | 2 |
| • BCD, Gray codes, alphanumeric representation in ASCII codes. | 2 |
| • Positive and Negative Logic, Basic Logic gates (NOT, OR, AND) & derived gates (NAND, NOR, EX-OR) Symbol and truth table, | 4 |
| • Applications of Ex-OR gates as parity checker and generator | 2 |

BOS Members:

Ms. Nanda Ranade, (Subject Expert)

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Mr. Manoj Kukade, (Subject Expert)

Kukade

Mr. Prafulla Wadaskar, (Industry Expert)

Prafulla

Ms. Divya Jagannathan, (Alumni)

Divya

Ms. Swatee Sarwate, (Chairman)

Swatee

Ms. Anitha Menon, (Internal Faculty)

Anitha



| Unit 2: Boolean algebra and Karnaugh maps | No. of Lect.=14 |
|--|-----------------|
| • Boolean algebra rules and Boolean laws: Commutative, Associative, Distributive, AND, OR and Inversion laws, | 3 |
| • De Morgan's theorem, Universal gates | 3 |
| • Min terms, Max terms, Boolean expression in SOP and POS form, conversion of SOP/POS expression to its standard SOP/POS form | 4 |
| • Simplifications of Logic equations using Boolean algebra rules and Karnaugh map (up to 3 variables, K map with don't care condition) | 4 |

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*Nanda
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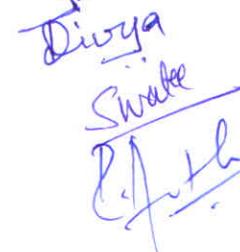
| Unit 3: Arithmetic Circuits | No. of Lect.=12 |
|---|-----------------|
| • Rules of binary addition and subtraction, subtraction using 1's and 2's complements | 2 |
| • Half adder, full adder, Half subtractor, Full subtractor, (circuit realization through k-map) | 6 |
| • Four bit parallel adder, Universal adder /subtractor, Digital comparator | 4 |

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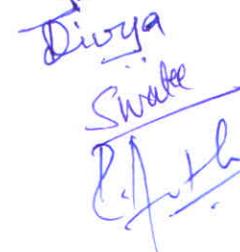

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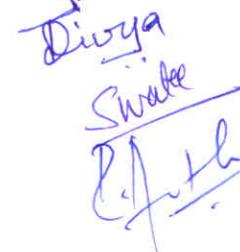

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